UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,871	09/09/2003	Min Yong Lee	CU-3356 RJS	2075

26530 7590 03/25/2005

LADAS & PARRY LLP
224 SOUTH MICHIGAN AVENUE
SUITE 1200
CHICAGO, IL 60604

EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,871	LEE ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities:

In line 12 of the claim, Applicant recites "in a portion of the gates in the semiconductor substrate". The examiner believes this should be replaced with –in a portion of the plurality gates of the semiconductor substrate–.

In line 14 of Claim 1, Applicants recited "implanting ion into". The examiner believes this should be replaced with –implanting ions into--.

In line 18 of Claim 1, Applicants recite "a activation temperature". The examiner believes this should be replaced with –an activation temperature--.

Claim 8 is objected to because of the following informalities:

In line 3 of claim 8, Applicants recite "as purge gas". The examiner believes this should be replaced with –a purge gas – since there has been no previous recitation of a purge gas. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 6-8, Applicants recite forming "a contact hole, which exposes a source/drain junction and a conductive layer in a portion of the gates in the semiconductor substrate". The examiner notes that Applicants invention forms more than one contact hole to expose the source/drain junction and a conductive layer in a portion of the gates in the semiconductor substrate. Further, there is no support for a single contact hole to expose both the source/drain and the conductive layer of the gate. The examiner suggests amending the claim to recite --selectively removing the insulation layer by using a first mask pattern to simultaneously form a contact hole which exposes a source/drain junction, and a contact hole that exposes a conductive layer in a portion of the gates of the semiconductor substrate-- .

Similarly, in line 20 of claim 1, Applicants recite "burying the contact hole". The examiner notes that since at least two contact holes are formed it is unclear which contact hole is buried.

Claim 1 recites the limitation "the p= source/drain junction" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "of dopant" in line 18. There is insufficient antecedent basis for this limitation in the claim. The examiner believes this could be overcome by amending at line 14 of claim 1, "implanting ion into" to state –implanting dopant ions into–.

In re claim 6, in line 2, Applicants recite wherein rotation is adjusted within four times. It is unclear what is meant by this recitation. Does this require that the implantation is rotated 0-4 times during implantation?

Claim 6 recites the limitation "wherein rotation" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (U.S. Patent No. 6,093,629) in view of Divakaruni et al. (U.S. Patent No. 6,727,540).

In re claim 1, Chen discloses a method of manufacturing semiconductor devices, comprising the steps of:

forming a plurality of gates (see Figure 1) on a semiconductor substrate; forming an insulation layer (50) on an entire surface of the semiconductor substrate to coat the plurality of gates;

selectively removing the insulation layer by using a first mask pattern (52) to form a contact hole, which exposes a source/drain junction (53) and a conductive layer in a portion of the gates (54) in the semiconductor substrate;

removing the first mask pattern (see column 4, lines 20-23) and forming a second mask pattern (62) on the selectively removed insulation layer, the second mask pattern exposing the p+ source/drain junction the semiconductor substrate (the examiner notes that 62 expose N+ regions but note that Chen teaches that the sequence may be reversed; column 5, lines 1-10);

implanting ion into the p+ source/drain junction in the semiconductor substrate by using the second mask pattern as a mask (see Figure 4 and column 4, lines 30-45);

removing the second mask pattern (see column 4, lines 40-45) and

burying the contact hole with conductive material to form a contact plug (60).

Chen does not disclose the method of annealing the wafer at an activation temperature range of dopant which is implanted in the ion implantation step. Divakaruni et al. disclose the method of annealing the wafer after implanting (see column 5, lines 20-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the wafer so activate the impurity dopants in order to allow for lower resistivity and a better electrical connection.

Further, the examiner notes that while Chen discloses a contact plug, Chen does not disclose wherein the contact is to form a bitline contact plug. Divakaruni et al. disclose a contact plug connected to a source/drain region formed of metal or polysilicon that is used as bitline a contact plug. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the contact plug of

Chen as a bitline contact plug since the contact plug of Chen is capable of being a bitline contact plug that would allow for further integration.

In re claims 2 and 3, Chen teaches a ion implantation step performed with a dose of $2x10^{15}$ atoms/cm^2, and a energy of 30 keV (see column 4, lines 30-45), but does not specifically teach the method wherein the implant step is performed with a dose of $4.5x10^{15}$ atoms/cm^2, and a energy of 24 keV. The examiner notes that Applicant does not teach that the implant dosage range or the energy of implant range solve any stated problem or are for any particular purpose. Therefore, the dose and energy of implantation lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the implantation at a dose of $4.5x10^{15}$ atoms/cm^2, and a energy of 24 keV, since the method would perform equally well when the implantation occurs at different dosage and energy to create a doped source/drain region for electrical connection, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claims 4 and 5, Chen discloses the method wherein a tilt angle is adjusted in a range of about 0 to 60 degrees or between 0 and 90 degrees in the ion implantation

step (Chen shows 0 degrees from the direction normal to the substrate, or 90 degrees from the direction parallel to the substrate, from see Figure 4).

In re claim 6, Chen disclose the method wherein a rotation is adjusted within four times in the ion implantation step (Chen discloses a rotation of zero times, and is considered by the examiner to be within four times).

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (U.S. Patent No. 6,093,629) and Divakaruni et al. (U.S. Patent No. 6,727,540) in view of Sung et al. (U.S. Patent No. 6,124,178).

In re claims 7-8, Chen and Divakaruni et al. disclose the method as claimed and rejected above, but do not disclose the particulars of the rapid thermal annealing (RTA) including performing the RTA at 830 °C or less and wherein the RTA uses 1 to 25 slm N_2 gas as a purge gas.

Sung et al. disclose the method of performing a RTA at 830 °C or less and wherein the RTA uses 1 to 25 slm N_2 gas as a purge gas (see column 4, lines 27-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the RTA at 830 °C or less and wherein the RTA uses 1 to 25 slm N_2 gas as a purge gas because as Sung et al. teaches these conditions allow for activation of the dopants as well as reduction of structure stress and prevention of possible delamination.

In re claim 8, Chen, Divakaruni et al. and Sung et al. disclose the method as claimed, but do not teach the heating rate of 10 to 100 degrees C per second. The examiner notes that Applicant does not teach that the heating rate range solves any stated problem or is for any particular purpose. Therefore, the heating rate range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the RTA at a heating rate range of 10 to 100 degrees per second, since the method would perform equally well when the RTA occurs at different heating rate to activate the dopants of the source/drain and create an electrical connection, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk